Field-Effect Thermoelectric Hotspot in Monolayer Graphene Transistor

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Graphene is a promising candidate for the thermal management of downscaled microelectronic devices owing to its exceptional electrical and thermal properties. Nevertheless, a comprehensive understanding of the intricate electrical and thermal interconversions at a nanoscale, particularly in field-effect transistors with prevalent gate operations, remains elusive. In this study, nanothermometric imaging is used to examine a current-carrying monolayer graphene channel sandwiched between hexagonal boron nitride dielectrics. It is revealed for the first time that beyond the expected Joule heating, the thermoelectric Peltier effect actively plays a significant role in generating hotspots beneath the gated region. With gate-controlled charge redistribution and a shift in the Dirac point position, an unprecedented systematic evolution of thermoelectric hotspots, underscoring their remarkable tenability is demonstrated. This study reveals the field-effect Peltier contribution in a single graphene-material channel of transistors, offering valuable insights into field-effect thermoelectrics and future on-chip energy management.

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1. Introduction

The application of two-dimensional (2D) materials in thermoelectrics has received extensive attention.[1–3] Compared with traditional bulk materials, 2D materials have unique advantages considering thickness, mobility, and design flexibility.[4] As the most widely studied 2D material, graphene offers high carrier mobility and excellent thermal conductivity, making it an excellent nanoscale material for exploring power dissipation and thermal management.[5,6] Usually, the physical phenomena related to thermal distribution involve two effects, Joule heating[7] and the Peltier effect.[8] The Peltier heat flow ($\dot{Q}_{\text{Peltier}}$) is proportional to current (I) and Peltier coefficient (Π) by $\dot{Q}_{\text{Peltier}} = \Pi \times I$, where Π is equal to the product of the Seebeck coefficient (S) and temperature (T), as dictated by the Thomson relation,[9] based on a local thermal equilibrium assumption. Cooling/heating effect is determined by the sign of the net $\dot{Q}_{\text{Peltier}}$ ($\Delta\dot{Q}_{\text{Peltier}}$) accumulation. In a conventional thermoelectric device, the Peltier cooling/heating effect is predicted to appear at the heterojunction of dissimilar materials having different S (such as metal–graphene heterostructure).[10,11] The net Peltier flow $\Delta\dot{Q}_{\text{Peltier}}$ is determined as $\Delta\dot{Q}_{\text{Peltier}} = S_{\text{AB}} \times T \times I$, where $S_{\text{AB}} = S_{\text{A}} - S_{\text{B}}$ is the difference between the Seebeck coefficients of two materials. Recently, unconventional Peltier effects and related phenomena have been observed in single-material nanostructures, which have been explained by nanoconstriction-enhanced edge scattering, nanobubble-engineering-induced van der Waals barriers, and hot-electron-enhanced nonequilibrium thermoelectric effects.[12–14] Such intriguing thermoelectric effects in single-material devices have attracted tremendous research interest owing to their incorporation as an (electrically controllable) active method for the thermal management of semiconductor devices at the micro/nanoscale.

Based on an unique energy band structure and ambipolar characteristics,[15] field-effect gate operations enable electron and hole density tuning in the atomically thin channel by varying the gate voltage, resulting in an inhomogeneous distribution of channel conductance. Inhomogeneity causes spatial variations in electrothermal distribution, which is unique to carrier transport near the Dirac point. For example, representative studies[16,17] have adopted infrared emission microscopy to observe broad hotspots in graphene that can be directly assigned to the Dirac

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point. Numerous studies have investigated graphene characteristics near its charge neutrality point (CNP), including Dirac fermions, Dirac plasmons, Dirac magnetoplasmons, and Dirac fluids.[18–21] However, the current understanding of the energy dissipation mechanism related to Dirac hotspots is limited to irreversible electrothermal conversion, as dictated by classical Joule's law.[16,17] Nevertheless, the role of reversible thermoelectric interconversion phenomena such as the Seebeck and Peltier effects in the energy dynamics of Dirac hotspots remain unexplored, despite the distinctive thermoelectric properties of graphene.[2]

Herein, we use scanning thermal microscopy (SThM)[22] with nanoscale resolution to study the gate-controlled thermal effect in a monolayer graphene transistor and, for the first time, we compellingly establish the significant role of thermoelectric Peltier effect, along with Joule heating, in generating a Dirac hotspot. Both effects induce spatially local heating in the close vicinity of the CNP, aligning with the intuitive understanding of injected electron–hole recombination and jointly contributing to the observed localized hotspot confined within the small gated channel region. The unique local gate structure of highly thin hexagonal boron nitride (hBN) as the sandwiching dielectric layer not only improves the graphene quality with excellent charge transport properties free from defects or charge traps, but also enlarges the spatial gradient of the Seebeck coefficient owing to charge redistribution in the confined region, as defined by a small local gate length. Thus, the Peltier contribution is elevated. The device is in remarkable contrast to previous back-gate devices that have thick SiO_2 dielectric layer and a substantially larger channel length, defined by the distance between the source and drain electrodes.[10,16] In addition, electron–hyperbolic phonon coupling[23] in our encapsulated hBN–graphene–hBN device can improve the substrate cooling efficiency of the current-bearing device, favoring our experimental observation of local Dirac hotspots. The existence of the Peltier effect is demonstrated by comparing the simulated total lattice temperature and extracted Joule heating. Thus, the Peltier effect not only enhances but also localizes Dirac hotspots within the gated region. By biasing the local gate, the spatial shift of the Dirac hotspot along the channel becomes consistently observable, owing to its more localized nature. The results of this study provide insights into electrothermal/thermoelectric interconversion in actual graphene devices and offer clues for the active thermal management of future post-Moore nanoelectronics.

2. Results and Discussions

A schematic of the graphene transistor and the experimental nanothermometric imaging setup are shown in **Figure 1a**. The device comprises two graphene flakes and two hBN flakes deposited on a SiO_2/Si substrate by mechanical exfoliation. Bottom monolayer graphene (Gate-Gr) is used as a back gate electrode, hBN-2 flake of thickness ≈20 nm serves as a dielectric layer, top monolayer graphene (Channel-Gr) is the channel material of the device, and top hBN-1 of thickness 10 nm is transferred as a cover layer to encapsulate the device[24] (Figure S1, Supporting Information). Gate-Gr and Channel-Gr are perpendicular to each other, and the gate width (≈6 μm) is ≈1/3 of the Channel-Gr length. The local electrostatic gate can efficiently modulate charge distribution and transport in the graphene channel above

it. Figure 1b presents an optical microscopy (OM) image of the device. The black box in Figure 1b presents the channel region under measurement by SThM and contains two flakes of monolayer graphene material for the channel and gate layers. The heterostructure is revealed by micro-Raman mapping of intensity ratio between the 2D and G peaks (Figure 1c). The ratio I_{2D}/I_G in Channel-Gr is greater than five, implying a monolayered channel graphene. In our SThM measurement, a square wave modulated bias V_{DS} alternating between zero and $+V_0$ or $-V_0$ is applied to the source–drain electrodes, while a dc voltage V_G is applied to the gate electrode. The temperature distribution in the graphene channel is monitored using an SThM probe and demodulated using the V_{DS} modulation frequency. The measured signal presents the temperature difference produced by the flowing current, such that $\Delta T_L \equiv T|_{V_{DS} = +/-V_0} - T|_{V_{DS} = 0}$, where $T|_{V_{DS} = +/-V_0} (T|_{V_{DS} = 0})$ represents the temperature with (without) the source–drain bias. The demodulation technique significantly improves the temperature resolution by more than 10 mK.[22] The thermal distribution, as shown in Figure 1d, can arise from the net contribution of both electrothermal Joule[16,17] and thermoelectric Peltier[12,13,22] effects, which turn highly intense in the channel region.

Figure 2 shows the unique electrical and thermoelectric characteristics of a graphene transistor with hBN as the dielectric layer. The source–drain voltages with different amplitudes and directions can be tuned from −3 to +3 V at room temperature, as illustrated in Figure 2a. The drain current (I_D) peaks, marked by triangles, correspond to the CNP (V_{Dirac}) where the minimum channel currents are obtained. The local back gate V_G provides minimal density and current saturation in the gated region within the range of −2 to +2 V, an order of magnitude lower than the gate voltage of traditional substrate-back-gate devices using SiO_2 as the gate dielectric.[25,26] The graphene transistor gate voltage is of the same order as the source–drain voltage, resulting in a non-negligible effect of V_{DS} on the potential distribution in the graphene channel. Thus, charge density is determined cooperatively by the gate and source–drain voltages with the Dirac voltage V_{Dirac} shifting consistently from $V_{Dirac} = -1.36$ V to $V_{Dirac} = +1.05$ V when V_{DS} increases from −3 to +3 V. The Dirac point shows a linear dependence with different V_{DS} (inset of Figure 2a). For zero source–drain biasing, $V_{Dirac} = -0.09$ V is obtained by linear extrapolation, suggesting that the channel graphene is lightly n-doped in the intrinsic regions with 7.5×10^{10} cm^{-2} density (Section S5, Supporting Information). The slope of the fitting line is 0.41, which correlates with the gated region geometry. The schematic on the left of Figure 2b shows the graphene channel, where the bottom is grounded and the blue region represents the gated region with the center located at $x = 9$ μm. When V_{DS} is applied to the drain electrode, a linear electric potential $V_{channel}(x)$ is developed across the channel. When the graphene gate electrode under the channel is treated as an equipotential body, the local gate voltage V_G is constant within the gated region. We define $V_G^* = V_G - V_{Dirac}$, as indicated by the blue line. The crossover point of $V_{channel}(x)$ and V_G^* indicate the electrically neutral center of the gated region (Figure S4, Supporting Information). Notably, the ratio of V_G^* to V_{DS} is 9 μm/22 μm (≈0.41) based on the principle of similar triangles, and the slope of the fitting line matches in the inset of Figure 2a, validating the aforementioned Dirac transport scenario.

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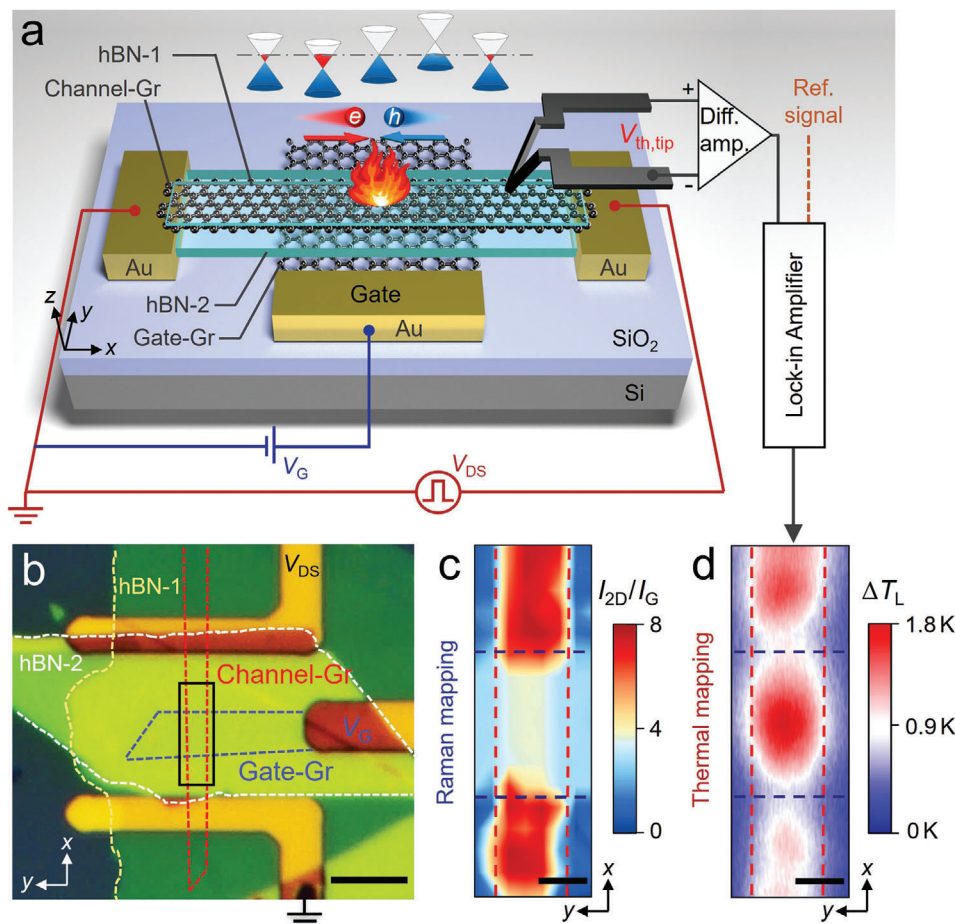
Figure 1. Nanoscale mapping of thermal distributions in the graphene transistor. a) Experimental set-up and schematic of the graphene transistor layout. The Dirac hotspot (marked by flame) in the graphene channel arises from the recombination of injected electrons and holes. b) Optical image of a graphene transistor. c) Raman mapping of I_{2D}/I_G ratio of the tested region marked by the black solid rectangle in (b). d) Experimental thermal distribution obtained with the input pulse $V_{DS} = 0$ to +3 V (AC) and $V_G = +1.05$ V (DC). Scale bar, 10 µm in (b), 2 µm in (c) and (d).

Within the gated region, the potential distribution is significantly influenced by the source–drain voltage as V_{DS} increases. At low bias, the carrier distribution in the channel is assumed to be relatively homogeneous. Therefore, the resistance of the gated region depends solely on its length, $R = R_{channel} \times L_{gate}/L_{channel}$. To obtain the effective electrical characteristic curve of gate-modulated graphene, excluding the resistance of the ungated intrinsic regions, we consider the transfer curve of $V_{DS} = 0.5$ V for effective calculation (Figure S5, Supporting Information). The local potential difference between $V_{channel}(x)$ and V_G^* is denoted as $V_G^{diff.}(x)$, such that

$$V_G^{diff.}(x) = V_G^* - V_{channel}(x) \quad (1)$$

The sheet resistance (R_S) is given by $R_S = R \times W_{gate}/L_{gate}$, where L_{gate} and W_{gate} are the length and width of the gated region, respectively. The R_S versus $V_G^{diff.}$ curve of the gated graphene is shown in Figure 2c, where R_S approaches its maximum value at $V_G^{diff.} = 0$, corresponding to the peak position for Joule heating. To calculate the Seebeck coefficient, we used the semi-classical Mott relation.[27] The validity of the Mott relation for this study

was based on the moderate charge mobility and disorder in our devices, both of which were comparable to those in previous studies.[28] According to the Mott relation, the Seebeck coefficient can be calculated using a transfer curve expressed as

$$S = -\frac{\pi^2 k_B^2 T}{3|e|} \frac{1}{G} \frac{dG}{dV_G} \sqrt{\frac{|e|}{C_g \pi}} \frac{2}{\hbar v_F} \sqrt{|V_G - V_{Dirac}|} \quad (2)$$

where k_B is Boltzmann's constant, e is the electron charge, $\hbar$ is the reduced Planck's constant, and v_F is the Fermi velocity. The gate capacitance $C_g = \epsilon_0 \epsilon_r/d$, where d is the dielectric hBN thickness. The measured G is the charge conductivity obtained from the transfer curve $I_D - V_G$. The peak value of the Seebeck coefficient attains ≈160 µV K^{-1}, which is similar to the values of graphene reported in previous studies.[12,27,29,30] The maximum slope of the $S-V_G^{diff.}$ curve is located at the CNP ($V_G^{diff.} = 0$), corresponding to the strongest Peltier heating position. The ungated R_S and S of the intrinsic regions are indicated by orange and green triangles in Figure 2c, respectively (left side of the vertical

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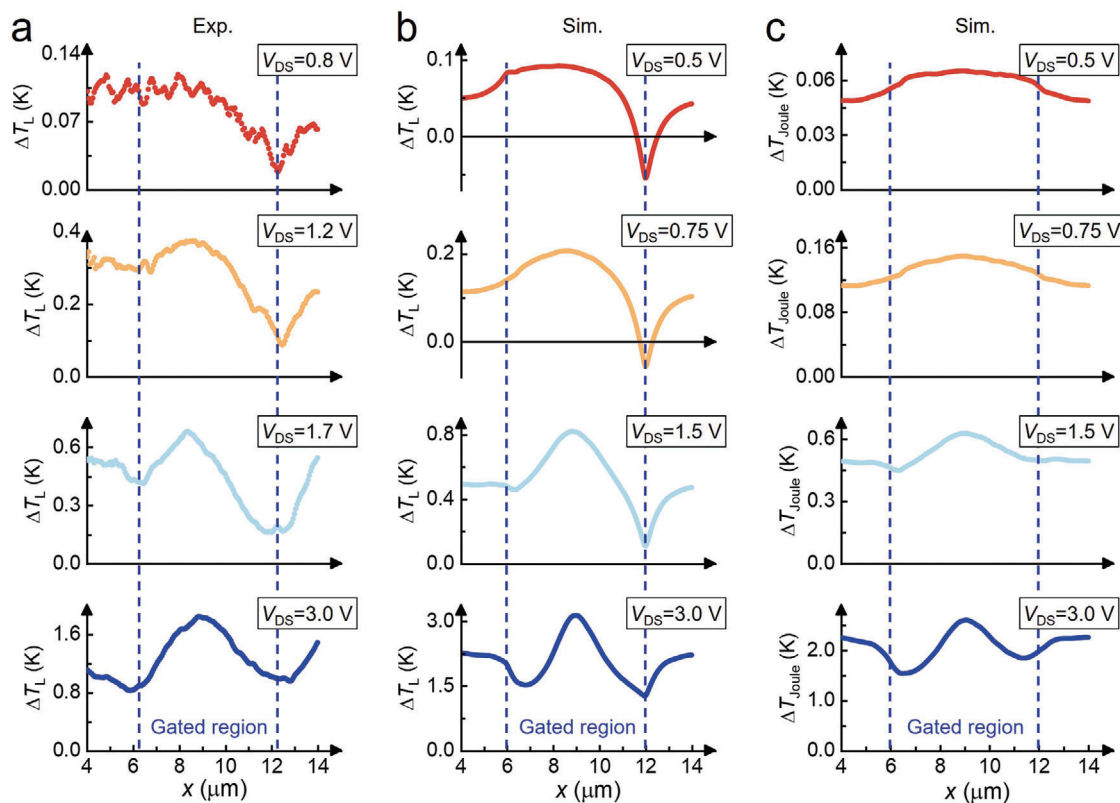
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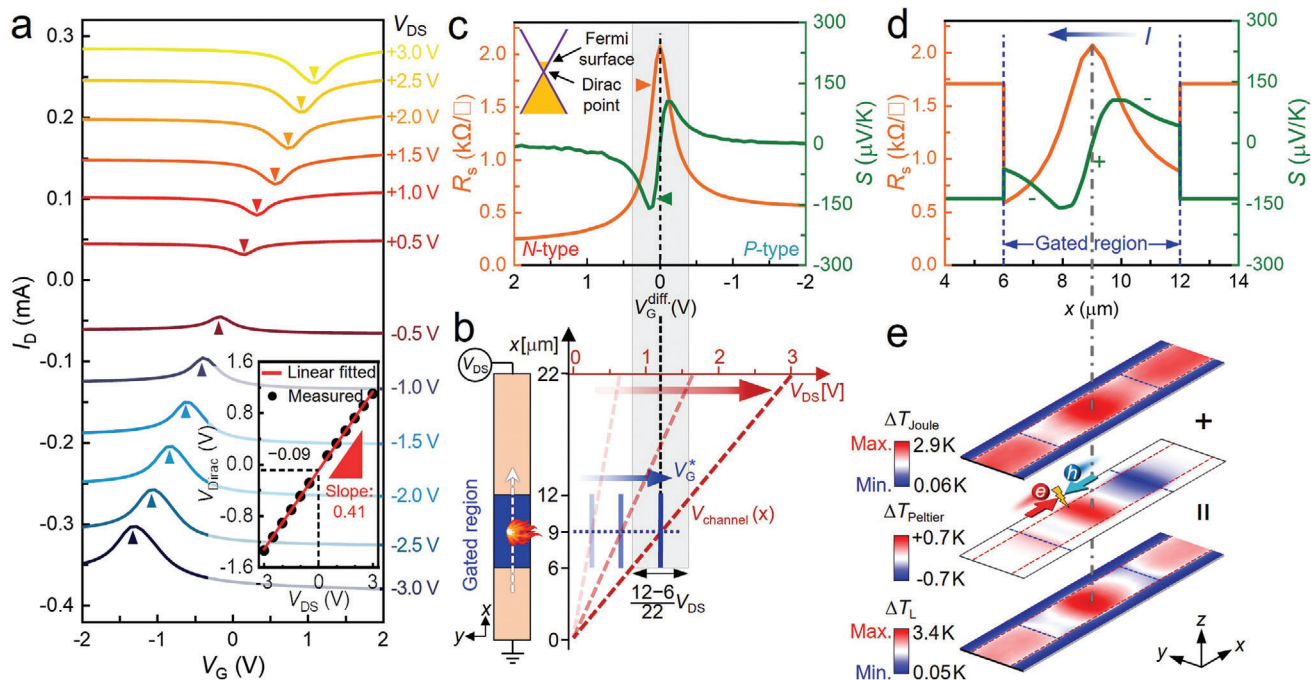
Figure 2. Electrical and electrothermal characteristics of a graphene transistor with distribution profiles of resistance and thermoelectric Seebeck coefficient in the gated region. a) Transfer characteristics of the graphene device with V_{DS} from −3 to +3 V. The position marked by arrows present the Dirac voltage V_{Dirac} at each V_{DS}. Inset: approximate linear dependence of V_{Dirac} on V_{DS}. The slope of the fitting line is 0.41. b) Diagram of potential distribution of the graphene channel with varying V_{DS}. Left: Schematic of graphene channel with gated region (blue). c) Sheet resistance R_S and Seebeck coefficient S as functions of $V_G^{diff.}$. Inset: Schematic of Fermi surface and Dirac point for lightly n-doped graphene in the intrinsic regions. d) Sheet resistance R_S and Seebeck coefficient S along the graphene channel at a fixed $V_{DS} = +3$ V. e) Simulated maps of Joule heating (top), Peltier effect (middle), and the total heat T_L (bottom) of graphene at $V_{DS} = +3$ V. ΔT_L is the sum of ΔT_{Joule} and $\Delta T_{Peltier}$.

dashed line), where the Fermi surface is slightly above the Dirac point (n-doped), as illustrated in the inset of Figure 2c.

With increasing source–drain voltage, a more significant effect of V_{DS} on the potential drop is observed compared to low-bias conditions. $V_G^{diff.}$ in the gated region under such conditions change, within the shaded region of Figure 2b,c, substantially varying with the spatial position along the graphene channel. The width of the shaded region ($\frac{12-6}{22}V_{DS}$) is determined by the width of the gated region and V_{DS}. Thus, the distributions of R_S and S as functions of position are shown in Figure 2d for $V_{DS} = 3$ V and $V_G = 1.05$ V. The net Peltier heat flow accumulation in the single graphene-material channel is $\Delta \dot{Q}_{Peltier} = -\nabla \dot{Q}_{Peltier} = -\nabla S \times T \times I$. Considering the current direction (marked in Figure 2d), a positive slope of the S curve corresponds to Peltier heating, while a negative slope corresponds to Peltier cooling. The maximum value of R_S–x and the slope of the S–x curves (the peak values of Joule and Peltier heating) are located concurrently at the center of the channel ($x = 9$ μm), where thermal concentration occurs in the gated region, both contributing to the Dirac hotspot. The total heat generated during electrothermal transport can be obtained by adding the contributions of the Joule and Peltier effects.[12,13] Figure 2e displays the simulated thermal mapping of ΔT_{Joule}, $\Delta T_{Peltier}$, and total ΔT_L in the identical region as shown in Figure 2d at $V_{DS} = +3$ V, where the scale bars for ΔT_{Joule} and ΔT_L are different in range from the $\Delta T_{Peltier}$ range, which reaches ≈50% of ΔT_{Joule}. The simulated ΔT_L mapping is in good agreement with the ex-

perimental mapping shown in Figure 1d at $V_{DS} = +3$ V, $V_G^* = +1.14$ V. Furthermore, the peaks of Joule and Peltier heating coincide at the center of the gated region, marked with grey dotted lines in Figure 2d,e. The Dirac hotspot of ΔT_L is more concentrated than that of ΔT_{Joule}, as the Peltier effect mapping is superimposed on the Joule mapping. Thus, Peltier heating enhances the peak temperature of Joule heating at the center of the channel for $V_{DS} = +3$ V, whereas Peltier cooling reduces the temperature near the hotspot edges, resulting in a more localized hotspot. The relatively strong Peltier effect is due to the large Seebeck coefficient gradient that arises from the local gate structure of the graphene transistor (van der Waals heterogeneously integrated graphene channel sandwiched between hBN layers) and the electronic Dirac cone band structure of graphene. As the maximum gradient of the Seebeck coefficient is located at the center of the gated region or the CNP, the confined electrons and holes converge and recombine generating heat, as shown in the mapping of $\Delta T_{Peltier}$ in Figure 2e (middle panel). Notably, the phenomenon is irrelevant to the Fermi surface position of the graphene channel as long as the Dirac point is attained in the gated region.

To investigate the evolution of thermal profiles in the gated region with varying bias voltages and weigh the Peltier effect contributions, the condition of $V_G^* = 0.41V_{DS}$ is maintained at different biases for pinning the Dirac point at the center of the gated region. **Figure 3a** presents the line profiles of the experimental ΔT_L signals for $V_{DS} = 0.8, 1.2, 1.7$, and 3.0 V. Owing to the asymmetric electrical characteristics of graphene

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Figure 3. Comparison between experimental and simulated temperature line profiles by tuning V_{DS}. a) Experimental line profiles of ΔT_L signals along the channel for V_{DS} = 0.8, 1.2, 1.7, and 3.0 V. b,c) Simulated line profiles of ΔT_L signals along the channel for V_{DS} = 0.5, 0.75, 1.5, and 3.0 V (b) with and (c) without the consideration of thermoelectric contribution. Seebeck coefficient in (b) is set according to Mott relation, while it is artificially set to be constant zero, resulting in pure Joule contribution in (c). V_G^* varies with V_{DS} in both experimental and simulated results, where $V_G^* = 0.41V_{DS}$.

transistors, pure Joule heating and the Peltier effect of devices are difficult to obtain separately using a single SThM measurement, as reported in previous studies.[10–14] To analyze the Peltier effect, we used numerical simulation and extracted the pure Joule heating contribution by artificially excluding the Peltier effect contributions (setting all Seebeck coefficients to zero). When the Peltier contribution is excluded, a pure Joule contribution is obtained, as shown in Figure 3c. Contrarily, the consideration of Peltier contribution by setting the Seebeck coefficient profile as in Figure 2c,d leads to the total heat distribution as shown by the ΔT_L profile in Figure 3b. A comparison of the experimental (Figure 3a) and simulated (Figure 3b,c) profiles provides compelling evidence confirming the existence of the Peltier effect. At low biasing conditions, the simulated temperature profile (top panel of Figure 3b) with the incorporation of Peltier contribution reproduces excellent overall tendency in the measured devices (top panel Figure 3a), as suggested by the obvious dip near $x \approx 12$ μm. Contrarily, the pure Joule profile exhibits nearly symmetrical distributions within the gated region (top panel of Figure 3c), which deviates from the experimental data. With increasing V_{DS}, the measured profile (Figure 3a) becomes consistent with the simulated data (Figure 3b), and both show an apparent peak at the Dirac hotspot position ($x = 9$ μm) when V_{DS} = 3.0 V. In addition, at highest biasing conditions of V_{DS} = 3.0 V (for instance, bottom panels of Figure 3a,c), the

difference between the measured and two simulated data becomes less prominent, suggesting a higher ratio of Joule contribution to the total heat. The observation is reasonable as the Peltier signal is linearly proportional to the electrical current, such that $\Delta T_{Peltier} \propto I$, while Joule heat increases more rapidly as $\Delta T_{Joule} \propto I^2$. Thus, the distinctive difference under low-biasing conditions is explained, highlighting the undisputed contribution of the Peltier effect. The rich evolution of the line profiles directly observed in our experiments may arise from the unique van der Waals stacked structure with a graphene channel encapsulated by hBN, having enhanced thermal conductivity compared to previous graphene devices based on SiO$_2$ (Section S7 and Figure S9, Supporting Information, present a simulation of broadened hotspots with thicker gate dielectric layers). The excellent thermal conductivity of hBN, which is 600 times higher than that of SiO$_2$, is responsible for a high thermal conductivity in graphene transistors.[23,31]

As the peaks of the Peltier effect and Joule heating always coincide, the Peltier effect enhances and localizes the Dirac hotspot in the gated region at V_{DS} = +3 V without changing its location. The position of the Dirac hotspot can be manipulated by adjusting the gate voltage, where the peaks of Joule and Peltier heating are always located at the same positions (Figure S6, Supporting Information). To study the gate-dependent evolution of the Dirac hotspots in the graphene channel, we maintain V_{DS} as a fixed
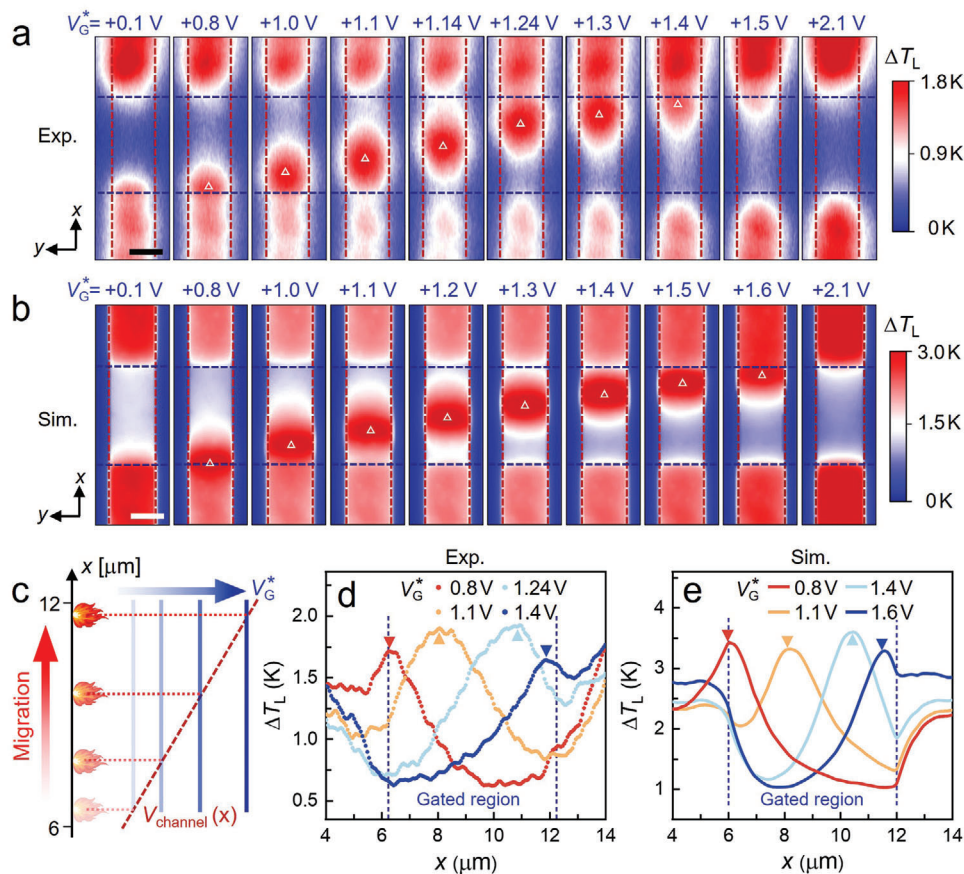
Figure 4. Dirac hotspot evolution manipulated by the gate voltage. a) Experimental thermal distributions with V_{DS} varying between 0 and +3 V (square wave), while V_G^* changes from +0.1 to +2.1 V. b) Simulated temperature distributions in the graphene channel under the same condition as (a). Scale bar, 2 µm in (a) and (b). c) Diagram of potential distribution along channel with varying V_G^* in the gated region. The flame (hotspot) shifts within the range of $x = 6$–12 µm (Gated region) as V_G^* increases. d) Experimental and e) simulated line profiles of ΔT_L along the graphene channel at different values of V_G^*.

square-wave alternating between 0 and +3 V while changing V_G^*. **Figure 4a** shows the measured ΔT_L maps along the graphene channel at different V_G^*. By varying V_G^* from +0.1 to +2.1 V, the hotspot appears at $V_G^* = +0.8$ V, shifts gradually from the lower edge of the gated region toward the upper edge, and eventually disappears at $V_G^* = +1.5$ V. Furthermore, a simulation with the incorporation of Peltier contribution (Figure 4b) reproduces the same features as in the experimental data, including the overall tendency of hotspot evolution with increasing V_G^* and thermal distributions under two extreme conditions ($V_G^* = +0.1$ V and $V_G^* = +2.1$ V). In the two extreme cases, the central hotspot disappears, and the gated region remains cooler than the intrinsic graphene beyond the gated region. To illustrate the migration of hotspots with varying V_G^*, Figure 4c displays schematically the potential distribution of the gated region. $V_{channel}(x)$ (dark red dotted line) increases along the channel, and its crossover point with $V_G^*(x)$ gives the position of the Dirac point. Hence, the hotspot location is obtained as indicated by the red dotted lines. With increase in V_G^*, the crossover points of V_G^* and $V_{channel}$ gradually shift upward, suggesting hotspot shifts in the gated region along the graphene channel. Figure 4d is obtained by extracting line profiles at $V_G^* = 0.8$, 1.1, 1.24, and 1.4 V from Figure 4a. In par-

allel, Figure 4e is obtained by extracting the corresponding line profiles at $V_G^* = 0.8$, 1.1, 1.4, and 1.6 V from Figure 4b. The reasonable agreement between the experimental and simulated line profiles along the channel, including the shape and shift of the hotspots in Figure 4d,e, implies the involvement of the Peltier effect under the local gate voltage. Notably, the excellent tunability of thermal distribution including the central hotspot evolution is highly reproducible in a parallel experiment, as shown in Figure S10 (Supporting Information).

In this study, the contribution of Peltier effect is observed, mainly for two reasons. First, the higher spatial and temperature resolutions of SThM, as compared to other techniques like noncontact and fast µ-Raman,[32] enable us to resolve the fine distribution of thermal signals from gate-defined small regions. Second, a high quality of the van der Waals heterogeneous integrated graphene channel sandwiched between the hBN layers significantly change the charge distribution and the Seebeck and Peltier coefficient distributions under local gate modulation, eventually allowing the Peltier contribution to be measured. Besides, we mention that including both Joule and Peltier effects turns out to be sufficient to explain our results, without introducing other effects like hot carrier effects.[33,34] This attributable

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to the low current density of our device compared with previous works.[12,33] and the multiple efficient cooling channels existing at room temperature.[3] In future studies, it will be interesting to explore the thermoelectric properties of high-quality graphene devices with hot carrier effect, or at low temperatures which allow perfect transmission of electrons due to pseudo-spin conservation,[35] or in the hydrodynamic transport region.[36–38] In hydrodynamic region, counterpropagating electrons and holes with opposite momenta form the quantum-critical Dirac fluid at the CNP (hotspot) with intriguingly new physical phenomena such as extraordinarily high conductance[39] (hence, suppressed Joule contribution), giant diffusivity,[40] and the breakdown of the Wiedemann–Franz law.[21]

3. Conclusion

This paper reports the direct control of hotspots with a considerable Peltier contribution in a single-graphene-material channel via local gate modulation, for the first time. The simulation results are in excellent agreement with the experimental data, confirming the existence of the Peltier effect. Furthermore, the Dirac hotspot shifts consistently in the gated region when the gate voltage is tuned. Our results reveal the thermoelectric properties of van der Waals materials, and offer a promising solution for on-chip energy management.

4. Experimental Section

Device Fabrication: The heterostructure of the hBN/graphene channel/hBN/graphene gate device was transferred using a stamp comprising polycarbonate (PC) and polydimethylsiloxane (PDMS) films. The PC film was obtained by dropping a PC solution (5 wt%) onto a glass slide. A PC sheet (3×3 mm) was scratched from the entire PC film and stuck onto a PDMS sheet (5×5 mm) on a glass slide, which was referred to as a stamp. The detailed transfer process is shown in Figure S1 (Supporting Information). After completion of the transfer process, the device was annealed at 250 °C in Ar/H_2 (200/10 sccm) for 2 h at a low pressure (≈ 80 Pa) to reduce the PC residue and improve contact between graphene and electrodes.

SThM: A passive SThM system was used to study the Joule heating and Peltier effect. The apparatus was placed in an ambient environment, and the spatial resolution was determined by the tip size of the thermocouple (≈ 50 nm). The device was subjected to an AC voltage V_{DS} through Cr/Au contacts at a frequency of $f_{exc} = 413$ Hz. During SThM measurement, the thermal signals collected by the tip were sent to a VertiSense imaging amplifier and demodulated using an SRS830 lock-in amplifier. The thermal signal ΔT_L was demodulated at the first harmonic (f). The lock-in measurements were performed following the method introduced by Harzheim[12] and Menges[22] to exclude tip samples and contact-related artifacts.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

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